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[The anatomy of the register file in a multiscalar processor - all 5 versions »](#)

SE Breach, TN Vijaykumar, GS Sohi - Proceedings of the 27th annual international symposium on ..., 1994 - portal.acm.org

... a task is committed. To avoid this multiple register copy operation ... and present register banks, somewhat similar to approaches proposed ...

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[Interrupt cascading and priority configuration for a symmetrical multiprocessing system - all 2 versions »](#)

J MacDonald, R Mahalingaiah - US Patent 5,568,649, 1996 - freepatentsonline.com

... software as well as a single copy of each ... to be a cascaded interrupt MSK Mask 1

Interrupt ... registers unit 650 includes a current task priority register 650A, a ...

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[Register window management for a real-time multitasking RISC](#)

DJ Quammen, DR Miller, D Tabak - System Sciences, 1989. Vol. I: Architecture Track, ..., 1989 - ieeeexplore.ieee.org

... in the fastest storage available, and not copy it at ... exploited in a multitask system

since task switches do ... to involve en masse copying of register values to ...

[Cited by 4](#) - [Related Articles](#) - [Web Search](#)

[\[PDF\] XMM-OM ICU FM SOFTWARE DETAILED DESIGN - all 2 versions »](#)

ESA PX, H Eggel, C Rochus, S Roose, UT Sasseen, M ... - mssis7.mssl.ucl.ac.uk

... This copy printed at 11:10 AM on 12-May-00 ... Added descriptions of a) task priority structure b) interrupt structure c) exception handling and debugging d) use ...

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[Series/1-An Architecture For The Future](#)

RE Birney, DG Bourke - COMPCON'77, 1977 - ieeeexplore.ieee.org

... composed of the Instruction Address Register, the Address Key Register, the Level ... primitive base for dispatching a task to a particular priority ...

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[\[CITATION\] The Anatomy of the Register File in a Multiscalar Processor](#)

SEBTV Gurindar, S Sohi - Proceedings of the 27th Annual International Symposium on ..., 1994 - Association for Computing Machinery (ACM)

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[\[PDF\] Exception and Interrupt Handling in ARM](#)

AFM Abdelrazek - iti.uni-stuttgart.de

... mode to user mode to protect link register from being ... The part of the task stack used in this ... between interrupts by priorities, so lower priority interrupt can ...

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[Integrated hardware and software task control executive - all 4 versions »](#)

JS Bronte - US Patent 6,061,709, 2000 - freepatentsonline.com

... the hardware executive interrupt or task can indirectly ... using the interrupt controller register to induce ... the software executive low priority interrupt routine ...

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[Method for conditional branch execution in SIMD vector processors - all 2 versions »](#)

RA Lorie, HR Strong Jr - US Patent 4,435,758, 1984 - [Google Patents](#)

... and controls added to the parallel task processor and ... 8 show apparatus for implementing register modification and ... ments required for enforcing priority ordering ...

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[Interrupt control architecture for symmetrical multiprocessing system - all 2 versions »](#)

D Gephardt, R Mahalingaiah - US Patent 5,555,430, 1996 - [freepatentsonline.com](#)

... software as well as a single copy of each ... to be a cascaded interrupt MSK Mask 1

Interrupt ... registers unit 650 includes a current task priority register 650A, a ...

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Key authors: [R Mahalingaiah](#) - [D Gephardt](#) - [A Federico](#) - [S Breach](#) - [J Wensley](#)



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